## REMARKS

Claims 1-19 remain pending in the present application. Claims 8 has been amended. Applicants have carefully and thoughtfully considered the Office Action and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

***Rejections under 35 USC § 103(a)***

1. On pages 2-6, in section 4, the Office Action, rejects claims 1-3, 8-9, 12, and 17-19 under 35 U.S.C. § 103(a) as being obvious over by H. Jonathan Chao and Li-Shen Chen, *Delay-Bound Guarantee in Combined Input-Output Buffered Switches*, GLOBAL TELECOMMUNICATIONS CONFERENCE, 2000. GLOBECOM '00. IEEE, November 27, 2000 – December 1, 2000, Vol. 1, pgs. 515-524 (hereinafter Chao) in view of U.S. Patent No. 7, 177,314 to Wu et al. (hereinafter 'Wu'). Applicants respectfully traverse the rejection.

Regarding claim 1, Chao and Wu, taken either singly or in any reasonable combination, do not disclose or suggest the claimed invention for at least the following reasons.

First, Chao does not inherently disclose or suggest "switch fabric having memory," as recited in claim 1. With respect to inherency, "[w]hen the PTO shows a sound basis for believing that the products of the applicant and the prior art are the same, the applicant has the burden of showing that they are not." In re Spada, 911 F.2d 705, 709 (Fed. Cir. 1990). Therefore, the prima facie case can be rebutted by evidence showing that the prior art products do not necessarily possess the characteristics of the claimed product. In re Best, 562 F.2d 1252, 1254 (CCPA 1977); *See also* MPEP 2112.01.

In contrast to claim 1, as Applicants discussed in their response to the Office Action of March 20, 2007, Chao discloses non-blocking switches with VOQs on the inputs. Chao, pg. 516, section III.A., right column. An exemplary design of a non-blocking switch is depicted in Figure 1 and the implementation of the SHLS scheme, as it applies to the non-blocking switch of Figure 1, is depicted in Figure 3. Chao, pg. 516, section III.A., right column, and pg. 519, section V., right column. **Figure 3 of Chao does not represent an exemplary switch architecture and therefore**

**cannot disclose a switch fabric**. Instead Figure 3 depicts communication between the various elements of the switch depicted in Figure 1. A cell is transmitted through the switch depicted in Figure 1 of Chao only after three steps are completed. First, based on the virtual finishing time of each individual packet, the IPC selects a packet from the input queue and sends a request to a corresponding output port. Chao, "Step 1: Selection and request," pg. 517 and "IPC operation:," pgs. 519 and 520. Second, the OAP selects an eligible packet from the IPC and sends a request to its corresponding input port. Chao, "Step 2: Grant," pg. 517 and "OAP operation:," pg. 520. Third, the IAP selects an eligible packet from the OAP with the smallest virtual finishing time. Chao, "Step 3: Accept," pg. 517 and "IAP operation:," pg. 521. The IAP then transmits the packet, comprised of cells, through the non-blocking switch to the corresponding output buffer. *Id.* **Therefore, as Chao does not disclose a need for the non-blocking switch to store the packet as the packet is being transmitted, Chao does not necessarily and logically possess the characteristics of claim 1.** In re Best, 562 F.2d at 1255; *See also* MPEP 2112.01. Chao, therefore, does not inherently teach a "switch fabric having memory," as recited in claim 1.

Furthermore, Wu fails to overcome the deficiencies of Chao. Wu discloses a crossbar used to move data from one bank of input RAM to another bank of output RAM. Wu, col. 5, l. 14-16. "The control of the data cross-over between the input RAM 16 and the output RAM 20 is determined by the copy machine 18 on a cycle-by-cycle basis." Wu, col. 5, l. 21-24. During every cycle, the crossbar moves a certain number of bytes (which is equal to the number of banks of input PAM) from the input RAM 16 to the output RAM 20. Wu, col. 5, l. 24-27. The transmission of bytes is therefore complete after each cycle. Therefore, as Wu does not disclose a need for the crossbar to store bytes as the bytes are being transmitted, Wu does not disclose or suggest a "switch fabric having memory," as recited in claim 1.

Second, on page 2 the Office Action states that "Chao does not disclose a controller that determines input priorities for cells from input queues and output priorities for cells from switch fabric to output queues." Applicant's agree.

Additionally, Wu fails to overcome the failings of Chao. Wu fails to disclose or suggest "**a controller determining input priorities for cells moving from said input queues to said switch fabric and output priorities for cells moving from said input switch fabric to said output**

queues," as recited in claim 1. In contrast, Wu discloses a transmit virtual concatenation processor (the "TVCP") used to process and transmit data from a system component to a transmission component. Wu, col. 3, l. 3-5. The TVCP is made of several components, including, a frame controller, a calendar, an input RAM, a crossbar, an output RAM, a copy machine, a reader, a terminator, and a provision database. Wu, col. 4, l. 13-17. The frame controller provides a master control function by orchestrating and managing all the components within the TVCP, including the crossbar, discussed above, and the copy machine. Wu, col. 4, l. 21-23. The copy machine causes data to be moved from the input RAM to the output RAM. Wu, col. 5, l. 49-50. The copy machine reads, maps, and writes data in accordance with a schedule RAM, programmed according to a schedule, located within the provisional database. Wu, col. 6, l. 2-4. The schedule, which remains static, contains channel mapping information which is used to control how the copy machine is to use the crossbar to read, map, and write data between the input RAM and the output RAM. Wu, col. 6. l. 7-15 and col. 8, l. 5-6. **Wu, therefore, discloses transferring bytes across the crossbar in accordance with a preexisting schedule**. Hence Wu does not disclose or suggest "a controller determining input priorities for cells moving from said input queues to said switch fabric and output priorities for cells moving from said input switch fabric to said output queues," as recited in claim 1.

Dependent claims 2 and 3 are allowable, at least, for being dependent from an allowable claim.

Regarding claim 8, Chao and Wu, taken either singly or in any reasonable combination, do not disclose or suggest the claimed invention for at least the following reasons.

First, Chao and Wu, taken either singly or in any reasonable combination, do not disclose or suggest "switch fabric having memory," as recited in claim 8 and discussed above in connection with claim 1.

Second, on page 4 the Office Action states that "Chao does not disclose a controller that determines input priorities for cells from input queues and output priorities for cells from switch fabric to output queues." This phrase does not appear in claim 8. In the event the Office Action intended to state that "Chao does not disclose a controller transferring highest priority cells in said switch fabric from said switch fabric to said output queues, transferring highest priority cells available for transfer in said input queues from said input queues to said switch fabric, prioritizing

arriving cells in said input queues based on times of said arriving cells to depart, and updating cells in said input queues available for transfer to said switch fabric," Applicant's agree.

Additionally, Wu fails to overcome the failings of Chao. Wu fails to disclose or suggest "**a controller transferring highest priority cells in said switch fabric from said switch fabric to said output queues, transferring highest priority cells available for transfer in said input queues from said input queues to said switch fabric, prioritizing arriving cells in said input queues based on times of said arriving cells to depart, and updating cells in said input queues available for transfer to said switch fabric**," as recited in claim 8. In contrast, as was discussed above in connection with claim 1, Wu discloses a transmit virtual concatenation processor (the "TVCP") used to process and transmit data from a system component to a transmission component. Wu, col. 3, l. 3-5. The TVCP is made of several components, including, a frame controller, a calendar, an input RAM, a crossbar, an output RAM, a copy machine, a reader, a terminator, and a provision database. Wu, col. 4, l. 13-17. The frame controller provides a master control function by orchestrating and managing all the components within the TVCP, including the crossbar, discussed above in connection with claim 1, and the copy machine. Wu, col. 4, l. 21-23. The copy machine causes data to be moved from the input RAM to the output RAM. Wu, col. 5, l. 49-50. The copy machine reads, maps, and writes data in accordance with a schedule RAM, programmed according to a schedule, located within the provisional database. Wu, col. 6, l. 2-4. The schedule, which remains static, contains channel mapping information which is used to control how the copy machine is to use the crossbar to read, map, and write data between the input RAM and the output RAM. Wu, col. 6. l. 7-15 and col. 8, l. 5-6. **Wu, therefore, discloses transferring bytes across the crossbar in accordance with a preexisting schedule**. Hence Wu does not disclose or suggest "a controller transferring highest priority cells in said switch fabric from said switch fabric to said output queues, transferring highest priority cells available for transfer in said input queues from said input queues to said switch fabric, prioritizing arriving cells in said input queues based on times of said arriving cells to depart, and updating cells in said input queues available for transfer to said switch fabric," as recited in claim 8.

Dependent claims 9 and 12 are allowable, at least, for being dependent from an allowable claim.

Independent claim 17 recites subject matter that is similar to that recited in claims 1 and 8, which are allowable over Choa in view of Wu as discussed above. Therefore, claim 17 is allowable for the same reasons discussed above in connection with claims 1 and 8.

Dependent claims 18 and 19 are allowable, at least, for being dependent from an allowable claim.

2. On pages 6-8, in section 5, the Office Action, rejects claims 4, 5, 7, and 10 under 35 U.S.C. § 103(a) as being obvious over Chao in view of Wu and further in view of Chuang et al., *Matching Output Queueing with a Combined Input/Ouput-queued Swtich*, IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, Volume 17, pg. 1030-1039 (hereinafter Chuang). Claims 4, 5, 7, and 10 depend from claim 1 or 8 and, thus, are allowable, at least, as being dependent from an allowable claim.

3. On pages 8-10, in section 6, the Office Action, rejects claims 6, 11, 13, and 14 under 35 U.S.C. § 103(a) as being obvious over Chao in view of Wu and further in view of Rojas-Cessa et al., *CIXB-1: Combined Input-One-Cell-Crosspoint Buffered Switch*, 2001 IEEE WORKSHOP ON HIGH PERFORMANCE SWITCHING AND ROUTING, May 31, 2001, pg. 324-329 (hereinafter Rojas-Cessa). Claims 6, 11, 13, and 14 depend from claim 1 or 8 and, thus, are allowable, at least, as being dependent from an allowable claim.

4. On pages 10-11, in section 7, the Office Action, rejects claims 15 under 35 U.S.C. § 103(a) as being obvious over Chao in view of Wu and further in view of Zhang et al., *Service Disciples for Guaranteed Performance Service in Packet-Switching Networks,"* PROCEEDINGS OF THE IEEE, October 31, 1995, pg. 1374-1396 (hereinafter Zhang). Claim 15 depends from claim 8 and, thus, is allowable, at least, as being dependent from an allowable claim.

5. On page 11, in section 8, the Office Action, rejects claims dependent claim 16 under 35 U.S.C. § 103(a) as being obvious over Chao in view of Wu and further in view of Rojas-Cessa and

further in view of Zhang. Claim 16 depends from claim 8 and, thus, is allowable, at least, as being dependent from an allowable claim.

***Conclusion***

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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